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10/608,855	06/27/2003	Francesco Ciovacco	2110-47-3	8247

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,855	CIOVACCO ET AL	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *7,12,13,16-18,22,34-40 and 50-53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,14,15,19-21,23-33 and 41-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19-20 and 45-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (5,807,789).

Regarding claims 19-20, Chen et al. teach in figures 4-6 and related text a method comprising:

forming a trench in an unmasked area of a substrate, the trench having inclined walls with a substantially constant slope and with rounded top corners (column 2, line 55); and

filling the trench with a dielectric material, wherein forming the trench further comprises:

performing a first plasma etch; and performing a second plasma etch.

Regarding claims 45-46, Chen et al. teach in figures 4-6 and related text a process for forming trenches with an oblique profile and rounded top corners in a wafer, comprising the steps of:

through a first polymerizing etch, forming in a semiconductor wafer depressions delimited by rounded top corners (column 2, line 55); and

through a second polymerizing etch, opening trenches at said depressions;

characterized in that said second polymerizing etch is performed in variable

plasma conditions (column 2, line 60 to column 4, line 18), to form trenches with oblique profile having approximately a same constant angle relative to a surface parallel to a face of the wafer, wherein said step of forming said second polymerizing etch comprises varying an etching voltage between said plasma and said wafer (this step is inherent in Chen et al.'s device).

Claims 19-21, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).
Regarding claims 19-21, AAPA teaches in figures 7-10 and related text a method comprising:

forming a trench in an unmasked area of a substrate, the trench having inclined walls with a substantially constant slope and with rounded top corners; and

filling the trench with a dielectric material, wherein forming the trench further comprises:

performing a first plasma etch; and performing a second plasma etch, and

forming a depression in the unmasked area of the substrate, and

forming a first polymeric film 14 on the walls defined by the depression and a stop layer 12 under a resist layer 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-22, 24-33, 41-44 and 47-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 21, Chen et al. teach substantially the entire claimed structure, as applied to claim 19 above, including forming a depression in the unmasked area of the substrate, but except forming a first polymeric film on the walls defined by the depression and a stop layer under a resist layer.

AAPA teaches in figures 7-10 and related text forming a depression in the unmasked area of the substrate, and forming a first polymeric film 14 on the walls defined by the depression and a stop layer 12 under a resist layer 13.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first polymeric film on the walls defined by the depression and a stop layer under a resist layer, in Chen et al.'s device in order to simplify the processing steps of making the device by forming the device by a known conventional method.

Regarding claim 24, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place Chen et al.'s wafer in an etching chamber and

to supply a constant chamber voltage thereto, in order to form the device in a known processing location (an etching chamber).

Regarding claims 22 and 26, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Cl2 and N2 and a substance chosen in the group comprising CHFa,CH2F2 in the polymerizing etch in Chen et al.'s device, in order to improve the etching steps of making the device.

Regarding claims 32-33, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to fill Chen et al.'s trench with a silicon oxide by CVD, in order to simplify the processing steps of making the device by depositing a known dielectric material in a conventional deposition method.

Regarding claims 24-25, 27-31 and 44, Chen et al. teach filling the chamber with a plasma mixture of gases; setting the temperature, pressure and gas flow; setting a chamber voltage; setting a series wafer voltages; creating a series of etching voltages between the substrate and the plasma; removing portions of the substrate by parts in series; and depositing a second polymeric film on the walls by pads in series, wherein the plasma mixture of gases comprises mixing hydrogen bromide and oxygen, wherein a rate of depositing the second polymeric film increases as the absolute value of the etching voltages increase, wherein depositing the second polymeric film further comprises controlling the growth of the walls of the trench by the series of etching

voltages, wherein creating a series of wafer voltages further comprises setting the wafer voltage to 10 volts for a first thirty seconds, setting the wafer voltage to 20 volts for a second subsequent thirty seconds, and setting the wafer voltage to 30 volts for a third subsequent thirty seconds, exposing decreasing portions of the wafer; and keeping a slope of the walls of the trench substantially constant, wherein the slope the walls is at an angle between sixty-five and eighty-five degrees to a vertical, wherein the steps have different durations.

Regarding claims 41-43, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a non-uniform voltage step function being a discrete parabolic voltage function and a continuous parabolic voltage function in Chen et al.'s device in order to improve the device characteristics by using routine experimentation and optimization.

Regarding claims 47-49, Chen et al. teach substantially the entire claimed structure, as applied to claim 45 above, except stating increasing the etching voltage by a discrete-ramp voltage function having steps of constant duration. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to increase the etching voltage by a discrete-ramp voltage function having steps of constant duration in Chen et al.'s device in order to obtain the best device characteristics, subject to routine experimentation and optimization.

Claims 1-6, 8-11 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (5,807,789) in view of Lee et al. (6,287,938).

Chen et al. teach in figures 4-6 and related text a process for forming trenches with an oblique profile and rounded top corners, comprising the steps of:

through a first polymerizing etch, forming in a semiconductor wafer depressions delimited by rounded top corners (column 2, line 55); and

through a second polymerizing etch, opening trenches at said depressions;

wherein said second polymerizing etch is performed by varying plasma conditions (column 2, line 60 to column 4, line 18) around the semiconductor wafer to form trenches with oblique profiles having a substantially constant slope,

wherein said step of forming said second polymerizing etch comprises varying an etching voltage between a plasma around the wafer and said wafer (this step is inherent in Chen et al.'s device),

wherein said step of varying comprises increasing said etching voltage (this step is inherent in Chen et al.'s device),

wherein said second polymerizing etch is an HBr- and O2-based etch,

wherein said step of forming a first polymerizing etch and said step of forming a second polymerizing etch are performed using a masking structure,

wherein the process comprises the step of filling said trench with a dielectric material.

Chen et al. do not teach forming trenches having a substantially constant slope throughout substantially an entire sidewall of each trench.

Lee et al. teach in figure 3 and related text trenches having a substantially constant slope throughout substantially an entire sidewall of each trench.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form trenches having a substantially constant slope throughout substantially an entire sidewall of each trench in Chen et al.'s device in order to prevent residual stress concentration.

Regarding claims 4-6, Chen et al. and Lee et al. teach substantially the entire claimed structure, as applied to claim 1 above, except an etching voltage being a discrete-ramp voltage of steps of constant duration of approximately 30 seconds. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an etching voltage being a discrete-ramp voltage of steps of constant duration of approximately 30 seconds in prior art's device, in order to obtain the best device characteristics, subject to routine experimentation and optimization.

Regarding claim 8, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place prior art's wafer in an etching chamber and to supply a constant chamber voltage thereto in prior art's device, in order to form the device in a known processing location (an etching chamber).

Regarding claims 10-11, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Cl2 and N2 and a substance chosen in

the group comprising CHFa,CH2F2 in the polymerizing etch in prior art's device, in order to improve the etching steps of making the device.

Response to Arguments

Applicant argues that Lee teaches away from combining Chen et al. and Lee, because Chen et al. try to avoid a structure described by Lee as discussed in column 1, lines 20-28 of Chen et al.

Chen et al. teach in column 1, lines 20-28 the disadvantages of using trenches with steep sidewall profiles (>80 degrees) and sharp corners. Lee does not teach trenches with steep sidewall profiles (>80 degrees) and sharp corners. Lee teaches an advantages trench isolation having reduced residual stress concentration. Therefore, an artisan would be motivated to modify Chen et al.'s trench in view of Lee's teachings.

Applicant argues that Lee does not teach trenches with constant slope portions.

Figure 2 of Lee clearly depicts a trench having a substantially constant slope throughout substantially an entire sidewall (excluding the top rounded corners).

Applicant argues that prior art does not teach varying an etching voltage between said plasma and said wafer.

Chen et al. teach using at least two different etching voltages in a plasma etching process (column 3, lines 21-47). Therefore, Chen et al. teach varying an etching voltage between said plasma and said wafer, as claimed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660.

The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
7/17/06

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